CLAIMS

1. A method of manufacturing a semiconductor device, comprising:

(a) providing a silicon semiconductor body (2,4) having opposed first and second major surfaces (80,82) having a lower-doped region (4) at the first major surface above a higher doped region (2), the lower-doped region (4) and the higher doped region (2) both being doped to have a first conductivity type, the lower-doped region (4) having a lower doping than the higher doped region (2);

(b) defining a mask (6) having openings (9) on the first major surface (80);

(c) forming trenches (8) through the openings (9) in the mask, the trenches (8) extending from the first major surface (80) towards the second major surface (82) through the lower-doped region (4) towards the higher doped region (2);

(d) depositing a trench insulating layer (12,52) on the sidewalls and base of the trenches as well as the first major surface;

(e) removing the trench insulating layer (12,52) from the top of the sidewalls of the trenches adjacent to the first major surface leaving exposed silicon (14) at the top of the sidewalls of the trench; and

(f) growing silicon (18) selectively on the exposed silicon (14) to grow silicon at the top of the trenches and plugging the top of the trenches,

wherein the method further includes defining a structure (10,50,52,74) for depleting the lower-doped region (4) in an operating state of the semiconductor device to allow the lower-doped region (4) to support a voltage in that operating state.

2. A method according to claim 1 further comprising the step of doping the sidewalls (10) of the trenches (8) to have a second conductivity type opposite to the first conductivity type to form the structure for depleting the lower-doped region before depositing the trench insulating layer (12).

3. A method according to claim 1 or 2 further comprising:

(g) forming a body region (22) being semiconductor doped to be of second conductivity type opposite to the first conductivity type at or adjacent to the first major surface (80) and adjacent to the trenches (8).

4. A method according claim 3 further comprising the steps:

(h) forming a source region (24) of semiconductor doped to be of the first conductivity type at or adjacent to the first major surface (80) and in contact with the body region (22); and

(i) forming an insulated gate (28) for controlling conduction between source region (24) and higher doped region (2) acting as the drain through the body (22).

5. A method according to any preceding claim wherein step (e) comprises overetching to remove the trench insulating layer (12) from the base of the trenches (8) and the first major surface (80) as well as the top of the sidewalls of the trenches adjacent to the first major surface leaving the exposed silicon (14) at the top of the sidewalls of the trench and the base of the trenches.

6. A method according to any preceding claim further comprising the step of depositing semi-insulating polysilicon (50,74) on the sidewalls of the trenches to form the structure for depleting the lower-doped region.

7. A method according to claim 6 further comprising the steps, after step (c), of:

depositing an outer trench insulating layer (12) on the sidewalls of the trench and the top surface;

removing the outer trench insulating layer (12) from the base of the trench;

followed by the steps of depositing semi-insulating polysilicon (50) in the trench and then step (d) of depositing a trench insulating layer (52);

wherein step (e) of overetching includes one or more etching steps etching the outer insulating layer (12), the semi-insulating polysilicon (50) and the trench insulating layer (52) to expose the sidewalls of the trenches adjacent to the first major surface.

8. A method according to any preceding claim wherein in step (f):

silicon (70) is grown selectively on the exposed sidewalls (14) at the top of the trench leaving a gap between the silicon (70) grown on opposed sidewalls;

a silicon layer is deposited on the first major surface plugging the gap (72) in the trench;

and the silicon layer deposited on the first major surface is removed, leaving the silicon layer (74) plugging the gap (72).

9. A semiconductor device, comprising:

a silicon semiconductor body (2,4) having opposed first and second major surfaces (80,82) having a lower-doped region (4) above a higher-doped region (2), the lower-doped region (4) and the higher-doped (2) region both being doped to have a first conductivity type;

trenches (8) extending from the first major surface (80) towards the second major surface (82) through the lower-doped region (4) towards the higher doped region (2);

a silicon plug (18,72) plugging the top of the trenches above a void (20) in the trenches (8); and

a structure (10,50,52,74) for depleting the lower-doped region in an operating state of the semiconductor device to allow the lower-doped region to support a voltage in that operating state.

10. A semiconductor device according to claim 9 wherein the semiconductor adjacent to the sidewalls (10) of the trenches is doped to be of a second conductivity type forming the structure for depleting the lower-doped region.

11. A semiconductor device according to claim 9 or 10 further comprising a layer of semi-insulating polysilicon (52,74) extending along the sidewalls of the trenches forming the structure for depleting the lower-doped region, the semi-insulating polysilicon (52,74) being in electrical connection with the semiconductor under the trench and to the silicon plug at the top of the trench.

12. A semiconductor device according to any of claims 9 to 11, having an active region (32) and an edge termination region (34) around the active region, wherein a plurality of the trenches (8) form an edge termination structure in the edge termination region (34), edge body regions (36) doped to be of second conductivity type opposite to the first conductivity type extend between the trenches (8) in the edge termination region (34), and the silicon plugs (18) in the trenches in the edge termination region (34) are undoped to form a high-resistance path between the edge body regions (36) on either side of the trenches (8).

13. A semiconductor device according to claim 12 comprising a plurality of the trenches (8) plugged with a silicon plug (18) in the active region (32), the silicon plugs (18) in the trenches (8) in the active region (32) being doped to be conductive.

14. A semiconductor device according to any of claims 9 to 13 further comprising:

a body region (22) being semiconductor doped to be of second conductivity type at or adjacent to the first major surface and adjacent to the trenches; and

a source region (24) of semiconductor doped to be of the first conductivity type at or adjacent to the first major surface and in contact with the body region; and

an insulated gate (28) for controlling conduction through the body region (22) between the source region (24) and the higher-doped region (2) acting as a drain.

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